



LUNA | SERIAL INTERFACE BOARD

The LUNA is a PCI-based serial I/O card that supports both CCSDS (Conventional and Advanced Orbiting Systems) and time division multiplexed (TDM) data formats. The Luna also features a Reed-Solomon encoder/decoder to provide complete block error detection and correction for each of the CCSDS-recommended grades of service for Advanced Orbiting Systems (AOS).



Robust Capabilities at up to 30 Mbps

The LUNA input channel accepts serial data and clock at up to 30 Mbps and outputs frame data to the PCI bus. The input channel performs frame synchronization, de-randomization, CRC error detection, de-interleaving, Reed-Solomon error detection and correction, time-tagging, and quality annotation. The frame synchronizer control logic uses an adaptive strategy for acquiring frame synchronization which utilizes four acquisition states: Search, Check, Lock, and Flywheel. The input channel transfers annotated frame data to host computer memory for further processing. The LUNA output channel reads frame data from host computer memory via the PCI bus and outputs serial data and clock at up to 30 Mbps. The output channel performs Reed-Solomon encoding, interleaving, CRC encoding, pseudo-randomization, convolutional encoding, and error insertion.

Flexible Interface Options

The LUNA features a variety of serial interface options including TTL or RS-422 clock and data signals. Each LUNA card provides an internal clock, or inputs for external clock. The card provides user-programmable clock and data polarity. Ingenicomm manufacturer a wide variety of breakout and interface cables to meet the requirements for any installation.

Four main variants of the LUNA card are available:

- Rate-limited to 5 MHz with no Reed Solomon Encoding; female connector that is backward-compatible to the legacy MONARCH board
- Full rate capability at 30 MHz with Reed Solomon Encoding; female connector that is backward-compatible to the legacy MONARCH board
- SGLS ternary interface, rate-limited to 5 MHz with no Reed Solomon Encoding; male connector with binary, SGLS, and two-bit pin-out (software selectable)
- SGLS ternary interface with full rate capability at 30 MHz with Reed Solomon Encoding; male connector with binary, SGLS, and tow-bit pin-out (software selectable)

Key Features

- Frame synchronizer with automatic polarity correction
- TTL/RS-422 data and clock inputs supporting line rates up to 30 Mbps
- External clock reference input available
- 1-microsecond time tag resolution (requires external 10 MHz and 1 PPS strobe or auxiliary time board)
- PCM encoder/decoder supporting NRZ-L/S/M and BiΦ-L/S/M
- CCSDS pseudo-randomization and derandomization
- Optional Reed-Solomon encoder/decoder
- Optional ternary (SGLS) interface
- Optional data/enable interface

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LUNA Receiver

Frame Synchronizer

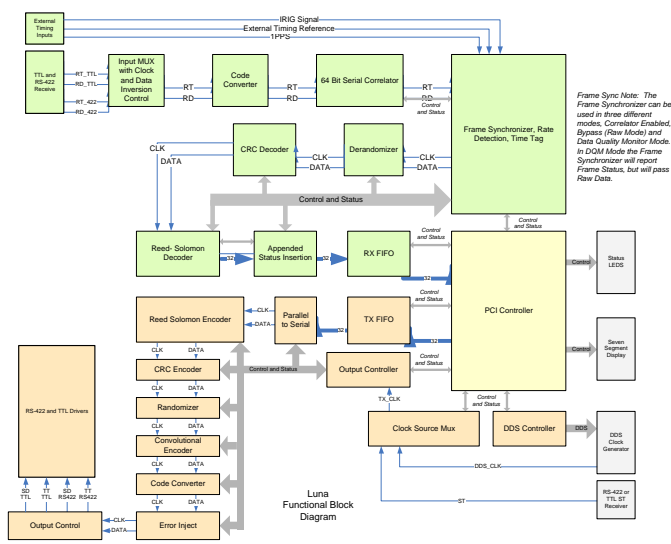
- Programmable frame sync pattern up to 64 bits
- Programmable frame sync mask up to 64 bits
- Programmable error threshold for acceptable sync patterns up to 15 bit errors
- Adaptive sync strategy with 0 to 15 check frames and 0 to 15 flywheel frames
- Programmable bit slip window from 0 to ± 3 bits
- Auto-polarity detection and correction
- Frame length up to 16,777,216 bytes/frame
- Operates in raw, correlator and DQM modes

Derandomizer

- Exclusive OR received frame data following sync pattern with pseudo-random pattern specified by CCSDS recommendations
- Shift register is initialized to all-ones pattern at the start of each frame
- Programmable start position

Reed-Solomon Decoder

- CCSDS Reed-Solomon (255,223) error correction
- Support for shortened code blocks using virtual fill
- Interleave depth from 1 to 15
- CCSDS Reed-Solomon (10,6) header error correction
- Real-time quality generation and annotation for each VCDU



LUNA Functional Block Diagram

LUNA Transmitter

Serial Output Logic

- Parallel-to-serial conversion
- CRC encoding
- Pseudo-randomization
- Convolution encoding
- Reed-Solomon encoding
- Command data formatting
- Bit error burst insertion at rates up to 30 Mbps
- Supports NRZ-L, NRZ-M, NRZ-S, BiΦ-L, BiΦ-M, BiΦ-S

Frequency Synthesizers

- Contains a Direct Digital Synthesizer (DDS) chip
- Direct digital synthesizer with output frequency from 0 Hz to 30 MHz, programmable in micro-hertz increments

Direct Digital Synthesizer (DDS) Chip

- Very high resolution frequency output from 0 Hz to 30 MHz
- An external reference can be used for higher transmit clock accuracy

Pseudo-Randomizer

- Exclusive OR frame data following sync pattern with CCSDS Recommended pseudo-random pattern
- Shift register is initialized to all-ones pattern at the start of each frame
- Programmable start position

Reed-Solomon Encoder

- CCSDS Reed-Solomon (255,223) encoding
- Support for shortened code blocks using virtual fill
- Interleave depth from 1 to 8

Convolutional Encoder

- Rate 1/2, constraint-length 7, convolutional code
- Connection vectors G1 = 1111001 and G2 = 1011011
- Programmable parity order and parity inversion

CRC Frame Error Control

- Compute frame error control field using the CCSDS polynomial
- Feedback shift register initialized to all-ones at each frame start
- Overlay computed CRC remainder into output frame
- Programmable start and end of included data

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