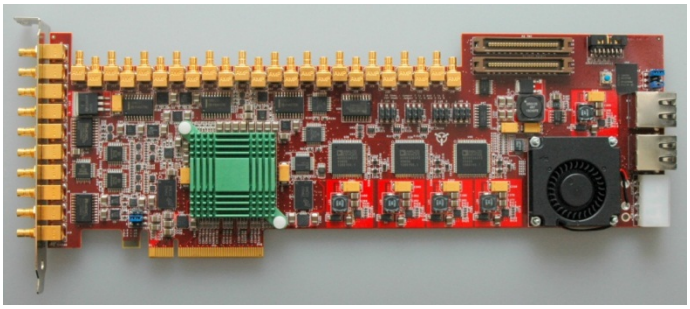
ORION | HIGH-RATE SERIAL INTERFACE BOARD

The ORION High-Rate Serial Interface Board is a PCI Express I/O card that supports both Conventional and Advanced Orbiting Systems (CCSDS) and Time Division Multiplexed (TDM) data formats. The Orion also provides Viterbi and Reed-Solomon decoding to provide complete bit and block error detection and correction for CCSDS-recommended grades of service for Advanced Orbiting Systems.



Full-Featured ECL Capability

The ORION input channel accepts NECL data and clock signals and outputs frame data to the PCI Express bus. The input channel performs Viterbi decoding, frame synchronization, de-randomization, CRC error detection, de-interleaving, Reed-Solomon error detection and correction, time-tagging, and quality annotation. The input channel transfers annotated frame data to host computer memory for further processing. The Orion output channel reads frame data from host computer memory via the PCI Express bus and outputs NECL data and clock signals.

The ORION can transmit and receive a clock and from 1 to 4 bits of data. The number of bits used is software selectable. All signals are differential NECL signals that are accessible on the back panel on SMB connectors.

Optional LVDS Interface

A LVDS daughterboard can be installed that will allow LVDS signals to be used in addition to the NECL signals. The daughterboard does not replace the NECL capability of the ORION card; it adds another user-selectable interface. For the receiver, adding the LVDS interface allows the user the ability to select either the NECL or the LVDS signals. On the transmitter, data can be simultaneously transmitted from both interfaces, LVDS and NECL.

Flexible Interface Options

The ORION is available in several convenient variants:

- 150 Mbps maximum rate with SMA or SMB connectors
- 450 Mbps maximum rate with SMA or SMB connectors
- 795 Mbps maximum rate with SMA or SMB connectors

Key Features

- Frame synchronizer with automatic polarity correction and dual correlators for QPSK data
- NECL interfaces with SMB connectors for reliable, high-speed I/O
- SMB outputs support rates up to 800 Mbps with an external clock reference
- Reed-Solomon and Viterbi encoder/decoder
- 1-microsecond time tag resolution with external 10 MHz and 1 PPS strobes or auxiliary time board
- PCM encoder/decoder supporting NRZ-L/S/M and BIΦ-L
- CCSDS pseudo-Randomization and de--randomization
- Optional LVDS interface

All boards are available with a bit synchronizer license operating up to 75 Mbps, as well as the optional LVDS transition module.

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ORION Receiver

Frame Synchronizer

- Programmable frame sync pattern and mask up to 32 bits in length
- Programmable error threshold for acceptable sync patterns
- Adaptive sync strategy with 0 to 7 check frames and 0 to 7 flywheel frames
- Programmable bit slip window from 0 to ± 3 bits
- Auto-polarity detection and correction
- Frame length up to 16,777,215 bytes/frame
- Dual correlators provide ambiguity resolution for QPSK data streams
- Correlator can be disabled to pass raw data

De-randomizer

- Exclusive OR received frame data following sync pattern with pseudo-random pattern given by $h(x) = x^8 + x^7 + x^5 + x^3 + 1$
- Shift register is initialized to all-ones pattern at the start of each frame
- Programmable start position

CRC Frame Error Detection

- Compute frame error control field from received data using the polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$
- Feed-back shift register is initialized to all-ones pattern at the start of each frame
- Programmable start and end of included data

Viterbi Decoder

- Rate = ½, k =7
- Programmable lockup parameters
- Programmable symbol swap and inversion
- Dual mode available for independent decoding of I and Q channels of a QPSK data stream.

Reed-Solomon Error Correction

- CCSDS Reed-Solomon (255,223) error correction
- Support for shortened code blocks using virtual fill
- Interleave depth from 1 to 8
- Real-time quality generation and annotation for each VCDU

Code Conversion

- Supports NRZ-L, NRZ-M, NRZ-S, BiΦ-L

Input Data Options

- Programmable input bit width
- 1-, 2-, or 4-bit input width
- 8-bit wide input possible with LVDS daughterboard
- Programmable data and clock polarity

Clock Regeneration

- The ECL input can accept data without a clock signal and detect and regenerate a clock for received data from 1 to 75 MHz

ORION Transmitter

Serial Output Logic

- Programmable clock and data polarity
- Frame length up to 16,777,216 bytes/frame

Convolutional Encoder

- Rate 1/2, constraint-length 7, convolutional code
- Connection vectors G1 = 1111001 and G2 = 1011011
- Programmable parity order and parity inversion
- Dual mode available for independent encoding of the I and Q channels on a QPSK data stream.

Frequency Synthesizers

- Onboard transmit clock generation 0 to 1428 MHz, adjustable in micro-Hertz increments

Code Conversion

- Supports NRZ-L, NRZ-M, NRZ-S, BiΦ-L

Re-Sequenced Output

- The re-sequenced output is a serial version of the multi bit input stream
- If QPSK mode is used on the receiver, this output can be enabled to transmit the QPSK stream as a recombined serial output stream

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